

MAR BASELIOS COLLEGE OF ENGINEERING AND TECHNOLOGY (AUTONOMOUS)
DEPARTMENT : ELECTRONICS AND COMMUNICATION ENGINEERING
Academic Year: 2024-2025 ODD SEMESTER

Class Time Table

Semester: S5 ECI		Room No: B109		Start date: 17/07/2024		End date: 21/11/2024					
Time	08:20-09:10	09:15-10:15	10:15-10:35	10:35-11:35	11:35-12:35	12:35-13:30	13:30-14:25	14:25-15:20	15:20-15:35	15:35-16:30	16:40-17:30
Day	1*	2	3		4	5		6	7		8*
Monday		IEFT	ADC	DSP(T)	DSP(T)	LUNCH		LIC(T)	AD(C)T		
Tuesday	MINOR	CS	SDP	SDP	SDP	H C H		DSP LAB (A) / AIC LAB (B)	DSP LAB (A) / AIC LAB (B)		
Wednesday	MINOR	DSP	LIC	ADC	ADC	B R R E A K		DSP LAB (B) / AIC LAB (A)	DSP LAB (B) / AIC LAB (A)		
Thursday	MINOR	ADC	LIC	CS	CS	A A K		DM	LIC		
Time	08:20-09:10	09:15-10:15	10:35-11:35	11:35-12:35	12:35-14:00	14:00-14:50	14:50-15:40	15:40-16:30	16:40-17:30		
Friday	MINOR	DM	DSP	IEFT	LUNCH BREAK	ADC	DSP	DSP	CS(T)		

*Periods 1 and 8 will be used for Honours/Minors/ Remedial/Extra Classes

Slot	Category	Course Code	Course Name	TT code	Faculty Name	Remarks
A	PCC	ECIU30A	Linear Integrated Circuits	LIC	Mr. SHERRY VARGHESE GEORGE	
B	PCC	ECIU30B	Digital Signal Processing	DSP	Dr VINEETHA MATHAI	
C	PCC	ECIU30C	Analog and Digital Communication	ADC	Dr. ANCY S. ANSELAM	
D	PCC	ECIU30D	Control Systems	CS	Ms. LAKSHMY S	
E	HSC	HSOU30A	Industrial Economics & Foreign Trade	IEFT	Mr.VINU V	
F	MNC	NC0U30A	Disaster Management	DM	Ms. ANN MARY ALEX	
S	PCC	ECIU38A	Analog Integrated Circuits and Simulation Lab	AIC LAB	Mr. SHERRY VARGHESE GEORGE/Ms. ANU SUSAN PHILIP	
T	PCC	ECIU38B	Digital Signal Processing Lab	DSP LAB	Dr VINEETHA MATHAI/Ms. GOURI NANDHANA	
M	VAC	MA0M30A	Random Process and Queuing Theory	MINOR	Ms. ANASWARA JOHNY & Ms. AKHILA MOHAN	B305B
	SDP		SDP - Simulink and PCB Design	SDP	Dr. LANI RACHEL MATHEW/Dr. ANCY S. ANSELAM	

Staff Advisor Details			
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